What is claimed is:

1. A timing recovery loop for generating adjusted timing pulses from a baseband signal waveform encoding a self clocking digital bit stream, the timing recovery loop comprising,

a pulse detector for generating data transition pulses from the baseband signal waveform, for comparing the data transition pulses with the adjusted timing pulses for generating early signals and lag signals

a random walk counter for counting the early signals and lag signals for generating a running count,

a threshold comparator for determining when the running count exceeds a predetermined threshold value, and

a timing pulse delay adjustor for delaying the adjusted timing pulses for synchronizing the adjusted timing pulses with the data transition pulses when the running count exceeds the predetermined threshold value.

2. The timing recovery loop of claim 1 further comprising,

a data detector for generating a reconstructed digital bit stream by sampling the baseband signal waveform by the adjusted timing pulses.

3. The timing recovery loop of claim 1 further comprising,

a threshold value selector for selecting the threshold value.

4. The timing recovery loop of claim 1 further comprising,

a threshold value selector for selecting the threshold value, and

an adaptive means for monitoring the rate at which the timing pulse delay is adjusted, the threshold value selector adaptively selecting different threshold values when the adjustment rate exceeds a predetermined rate.

5. The timing recovery loop of claim 1 further comprising,

a count magnitude generator for generating the magnitude count from the running count, the magnitude count being fed to the threshold comparator for determining when the running count exceeds the predetermined threshold value, and

a count sign clipper for generating a count sign from the running count, the count sign being fed to the timing pulse delay adjustor for generating a timing pulse delay to adjust the adjusted timing pulses, the sign count for increasing the timing pulse delay when the data transition pulses arrive late relative to the adjusted timing pulses and for decreasing the timing pulse delay when the data transition pulses arrive early relative to the adjusted timing pulses.

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6. The timing recovery loop of claim 1 wherein the pulse detector comprises,

a data transition pulse generator for generating the data transition pulses,

a timing delay for delaying reference timing pulses into the adjusted timing pulses, and

a lead and lag generator for generating lead and lag signals for early and late arrivals of the data transition pulses relative to the adjusted timing pulses.

7. The timing recovery loop of claim 1 wherein the pulse detector comprises,

a data transition pulse generator for generating the data transition pulses,

a timing delay for delaying reference timing pulses into the adjusted timing pulses, and

a data transition pulse counter for counting the number of data transition pulses within a search window following an adjusted timing pulse, and

a lead and lag generator for generating lead and lag signals for early and late arrivals of the data transition pulses relative to the adjusted timing pulses when one and only one data transition pulse occurs within each search window following an adjusted timing pulse.

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8. The timing recovery loop of claim 1 wherein the pulse detector comprises,

a data transition pulse generator for generating the data transition pulses,

a window delay for delaying the data transition pulses by half of a search window to center the data transition pulses within respective search windows,

a timing delay for delaying by a timing pulse delay the reference timing pulses into the adjusted timing pulses, the timing pulse delay being generated by the timing delay adjustor, the timing pulse delay being adjusted when the running count exceeds predetermined threshold value,

a data transition pulse counter for counting the number of data transition pulses within the search window following an adjusted timing pulse, and

a lead and lag generator for generating lead and lag signals for early and late arrivals of the data transition pulses relative to the adjusted timing pulses when one and only one data transition pulse occurs within a respective one of the search windows following a respective one of the adjusted timing pulses.

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